Modify note

Version	Date	Author	Change Note	Approved
V1			First edictor	

产品梦工厂

Title: Modify note

File: xSync

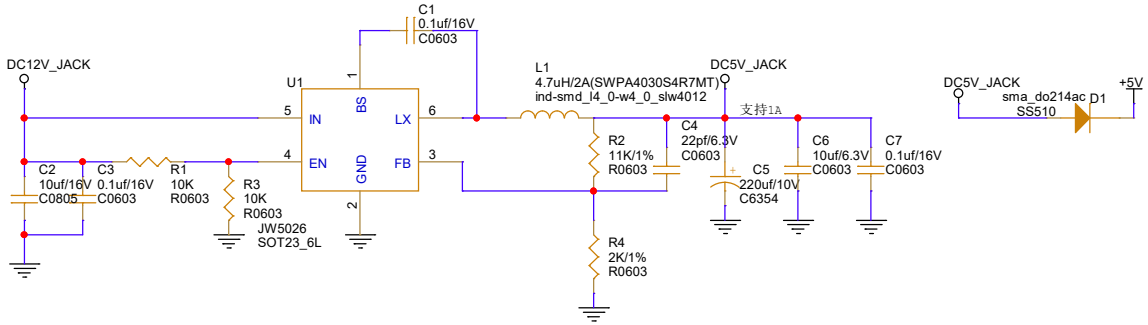
REV: v3

Create Date: Wednesday, October 11, 2023

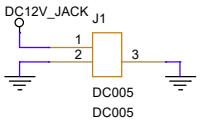
Page Num: 1

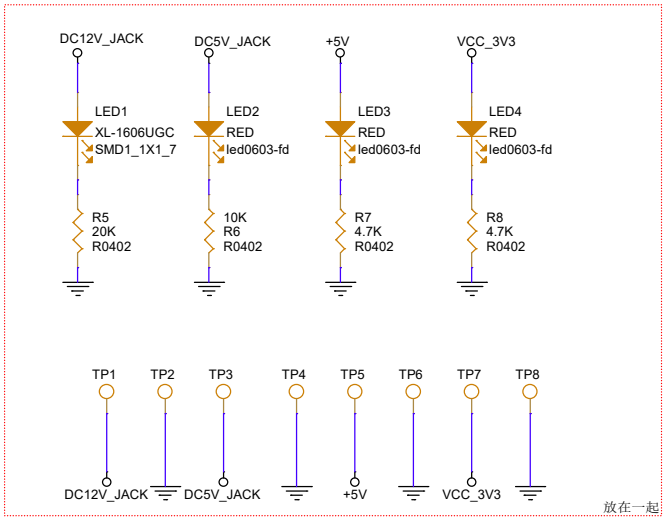
Modify Date:

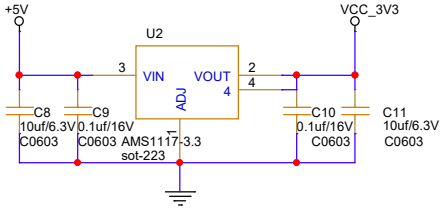
Page Total: 8



外部DC 12V供电

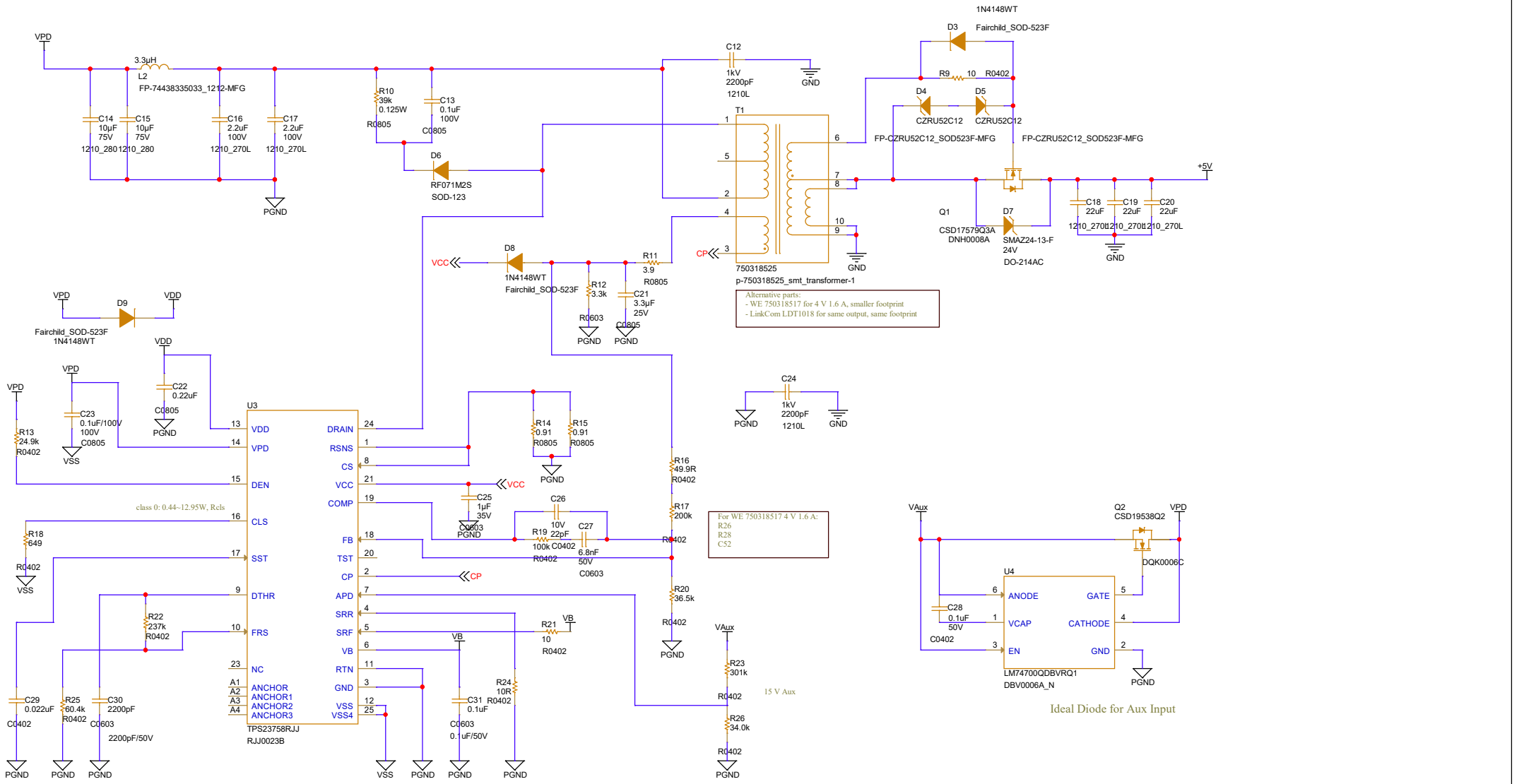


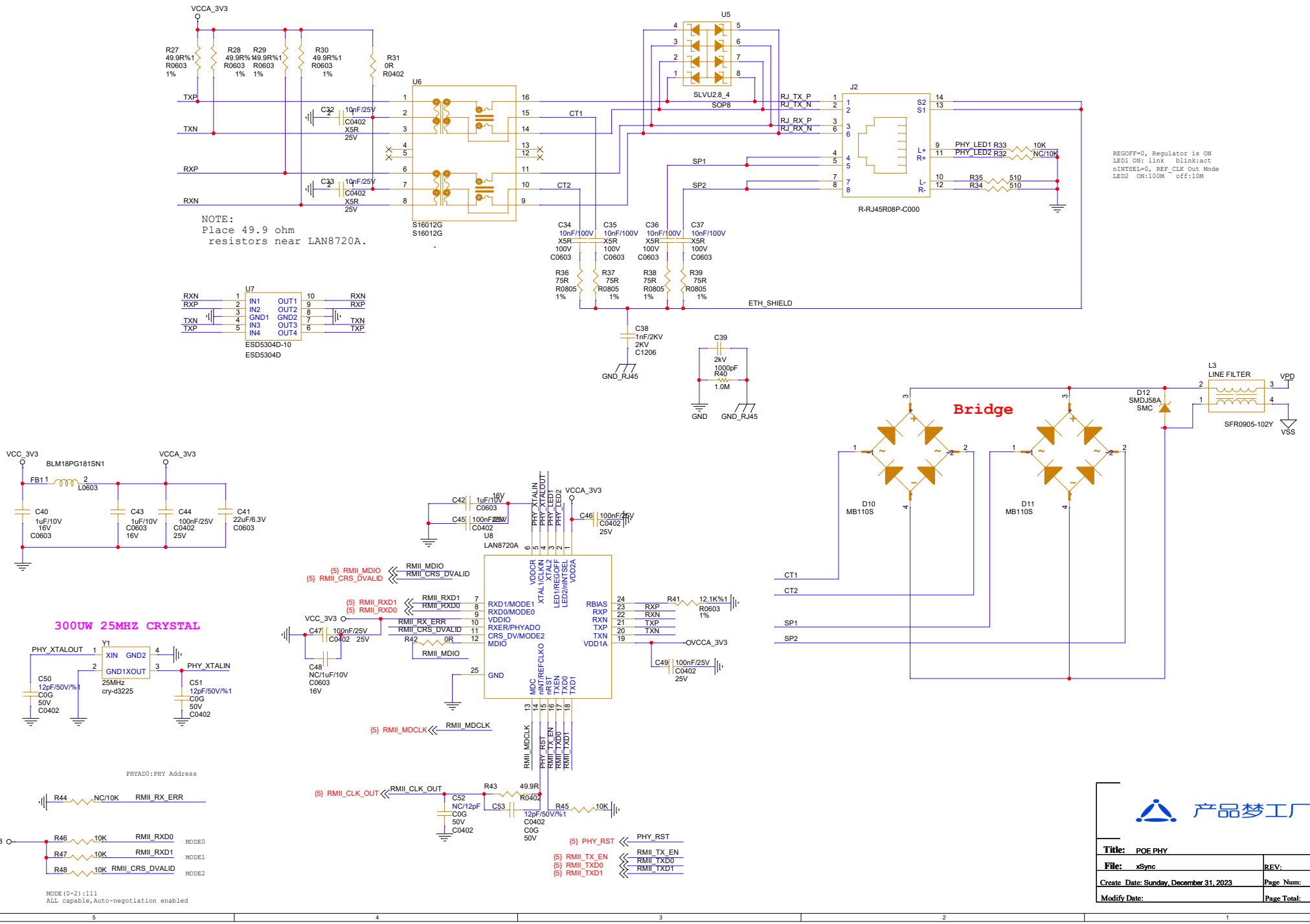


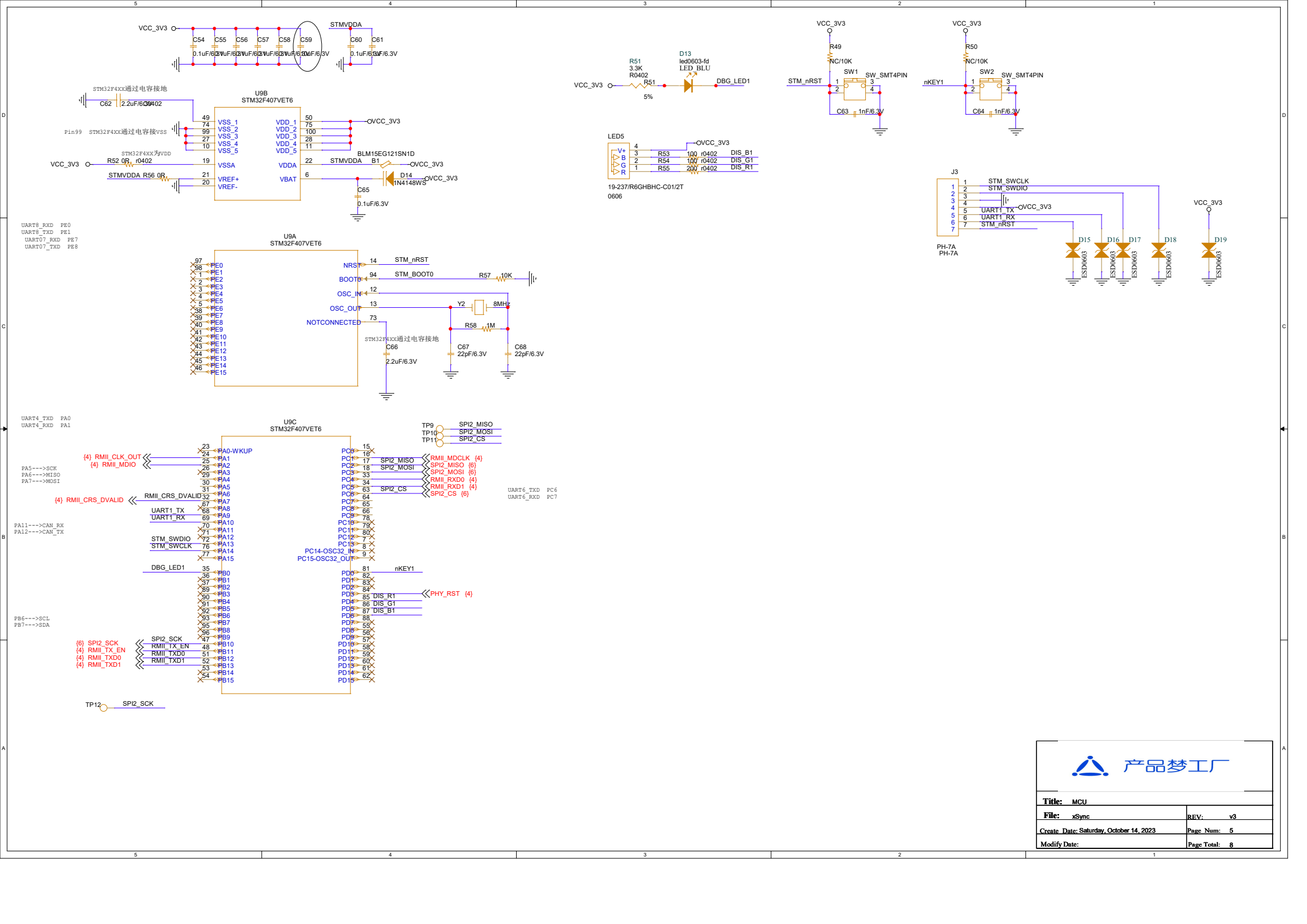


产品梦工厂

Title: POWER		
File: xSync	REV:	v3
Create Date: Wednesday, October 11, 2023	Page Num:	2
Modify Date:	Page Total:	8

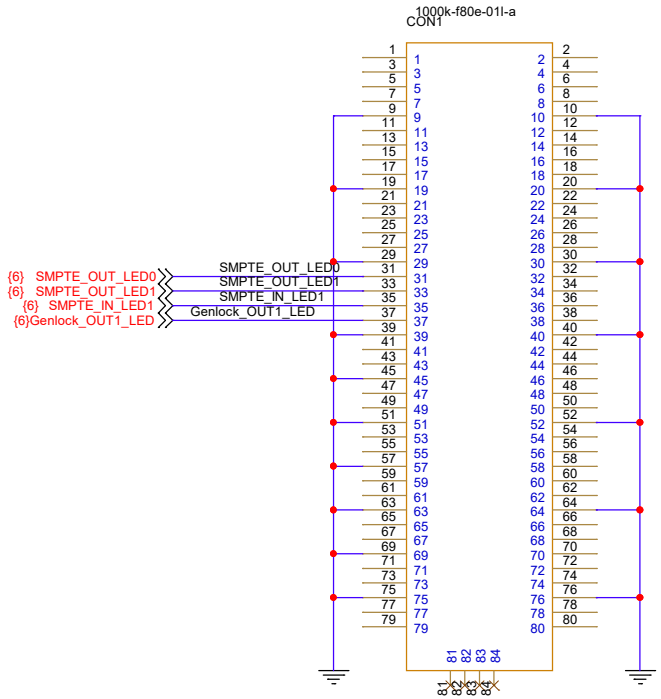

VPD
3.3µH
L2
FP-74438335033_1212-MFG
C14 10µF 75V 1210_280
C15 10µF 75V 1210_280
C16 2.2uF 100V 1210_270L
C17 2.2uF 100V 1210_270L
PGND
R10 39k 0.125W R0805
C13 0.1uF 100V C0805
D6 RF071M2S SOD-123
C12 1kV 2200pF 1210L
GND
1N4148WT
D3 Fairchild_SOD-523F
R9 10 R0402
D4 CZRU52C12
D5 CZRU52C12
FP-CZRU52C12_SOD523F-MFG
FP-CZRU52C12_SOD523F-MFG
T1
750318525
p-750318525_smt_transformer-1
+5V
Q1 CSD17579Q3A DNH0008A
D7 SMAZ24-13-F 24V DO-214AC
C18 22uF 1210_270L
C19 22uF 1210_270L
C20 22uF 1210_270L
VCC
D8 1N4148WT Fairchild_SOD-523F
R11 3.9 R0805
R12 3.3k R0603
C21 3.3µF 25V C0805
CP
Alternative parts:
- WE 750318517 for 4 V 1.6 A, smaller footprint
- LinkCom LDT1018 for same output, same footprint
VPD
D9
VDD
Fairchild_SOD-523F 1N4148WT
C22 0.22uF C0805
C23 0.1uF/100V 100V C0805
VSS
R13 24.9k R0402
U3
TPS23758RJJ
RJJ0023B
VDD
VPD
DEN
CLS
SST
DTHR
FRS
NC
ANCHOR
ANCHOR1
ANCHOR2
ANCHOR3
DRAIN
RSNS
CS
VCC
COMP
FB
TST
CP
APD
SRR
SRF
VB
RTN
GND
VSS
VSS4
class 0: 0.44–12.95W, Rcls
R18 649 R0402
R22 237k R0402
C29 0.022uF C0402
R25 60.4k R0402
C30 2200pF C0603 2200pF/50V
R14 0.91 R0805
R15 0.91 R0805
C25 1µF 35V C0603
C26 10V 22pF C0402
R19 100k R0402
C27 6.8nF 50V C0603
R16 49.9R R0402
R17 200k R0402
R20 36.5k R0402
R21 10 R0402
C24 1kV 2200pF 1210L
For WE 750318517 4 V 1.6 A:
R26
R28
C52
R23 301k R0402
R26 34.0k R0402
15 V Aux
VAux
Q2 CSD19538Q2 DQK0006C
U4 LM74700QDBVRQ1 DBV0006A_N
ANODE
VCAP
EN
GATE
CATHODE
GND
C28 0.1uF 50V C0402
R24 10R R0402
C31 0.1uF C0603 0.1uF/50V
Ideal Diode for Aux Input

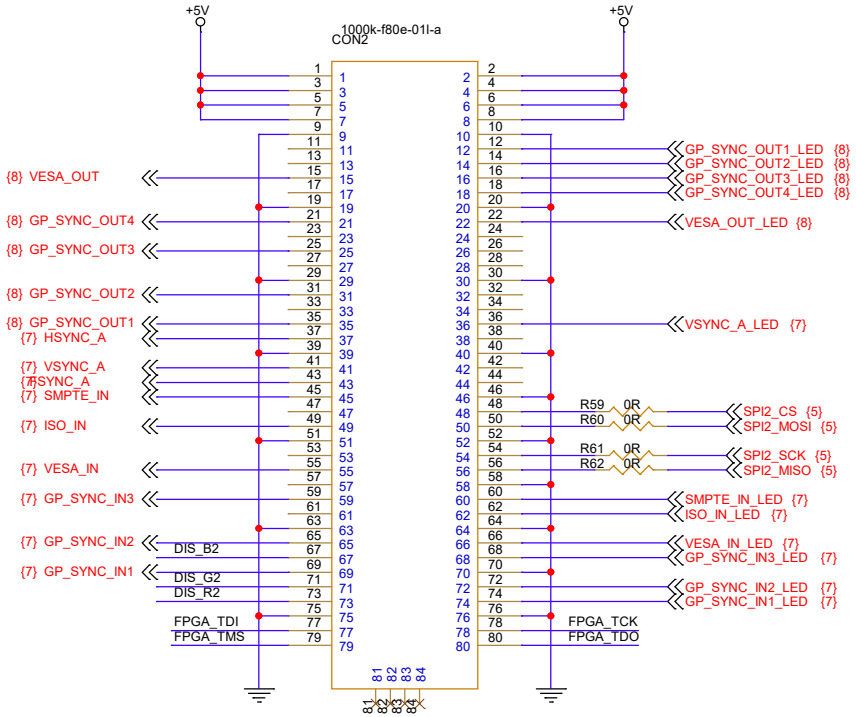

VCCA_3V3
R27 49.9R%1 R0603 1%
R28 49.9R% R0603 1%
R29 49.9R%1 R0603 1%
R30 49.9R%1 R0603 1%
R31 0R R0402
TXP
TXN
RXP
RXN
C32 10nF/25V C0402 X5R 25V
C33 10nF/25V C0402 X5R 25V
U6
S16012G
S16012G
CT1
CT2
U5
SLVU2.8_4
SOP8
RJ_TX_P
RJ_TX_N
RJ_RX_P
RJ_RX_N
J2
R-RJ45R08P-C000
SP1
SP2
PHY_LED1 R33 10K NC/10K
PHY_LED2 R32
R35 510
R34 510
REGOFF=0, Regulator is ON
LED1 ON: link blink:act
nINTSEL=0, REF_CLK Out Mode
LED2 ON:100M off:10M
NOTE:
Place 49.9 ohm
resistors near LAN8720A.
U7
ESD5304D-10
ESD5304D
C34 10nF/100V X5R 100V C0603
C35 10nF/100V X5R 100V C0603
C36 10nF/100V X5R 100V C0603
C37 10nF/100V X5R 100V C0603
R36 75R R0805 1%
R37 75R R0805 1%
R38 75R R0805 1%
R39 75R R0805 1%
ETH_SHIELD
C38 1nF/2KV 2KV C1206
GND_RJ45
C39 2kV 1000pF
R40 1.0M
GND
GND_RJ45
Bridge
D10 MB110S
D11 MB110S
D12 SMDJ58A SMC
L3 LINE FILTER
SFR0905-102Y
VPD
VSS
VCC_3V3
BLM18PG181SN1
FB1
L0603
C40 1uF/10V 16V C0603
C43 1uF/10V 16V C0603
C44 100nF/25V C0402 25V
C41 22uF/6.3V C0603
300UW 25MHZ CRYSTAL
Y1
XIN GND2
GND1XOUT
25MHz
cry-d3225
PHY_XTALOUT
PHY_XTALIN
C50 12pF/50V/%1 C0G 50V C0402
C51 12pF/50V/%1 C0G 50V C0402
C42 1uF/10V 16V C0603
C45 100nF/25V C0402
C46 100nF/25V C0402 25V
U8
LAN8720A
{5} RMII_MDIO
RMII_MDIO
RMII_CRS_DVALID
{5} RMII_RXD1
{5} RMII_RXD0
RMII_RXD1
RMII_RXD0
RMII_RX_ERR
RMII_CRS_DVALID
RMII_MDIO
C47 100nF/25V C0402 25V
C48 NC/1uF/10V C0603 16V
R42 0R
R41 12.1K%1 R0603 1%
C49 100nF/25V C0402 25V
OVCCA_3V3
{5} RMII_MDCLK
RMII_MDCLK
{5} RMII_CLK_OUT
RMII_CLK_OUT
R43 49.9R R0402
C52 NC/12pF C0G 50V C0402
C53 12pF/50V/%1 C0G 50V C0402
R45 10K
{5} PHY_RST
PHY_RST
{5} RMII_TX_EN
{5} RMII_TXD0
{5} RMII_TXD1
RMII_TX_EN
RMII_TXD0
RMII_TXD1
PHYAD0:PHY Address
R44 NC/10K RMII_RX_ERR
R46 10K RMII_RXD0 MODE0
R47 10K RMII_RXD1 MODE1
R48 10K RMII_CRS_DVALID MODE2
MODE(0-2):111
ALL capable,Auto-negotiation enabled
产品梦工厂
Title: POE PHY
File: xSync
REV: v3
Create Date: Sunday, December 31, 2023
Page Num: 4
Modify Date:
Page Total: 8



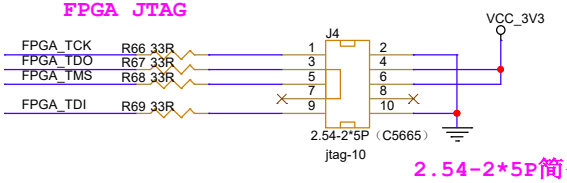
产品梦工厂

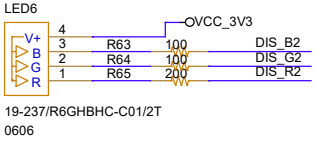
Title:	MCU		
File:	xSync	**REV:**	v3
Create Date:	Saturday, October 14, 2023	Page Num:	5
Modify Date:		Page Total:	8



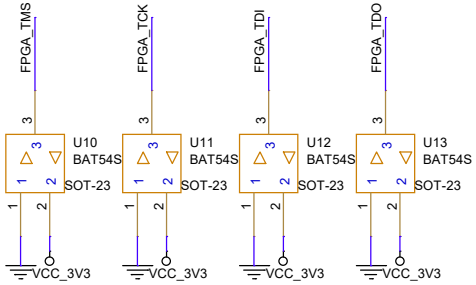


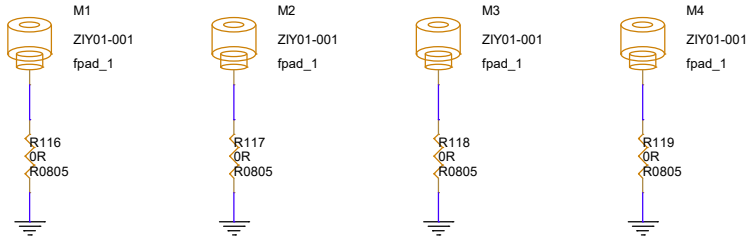
FPGA JTAG





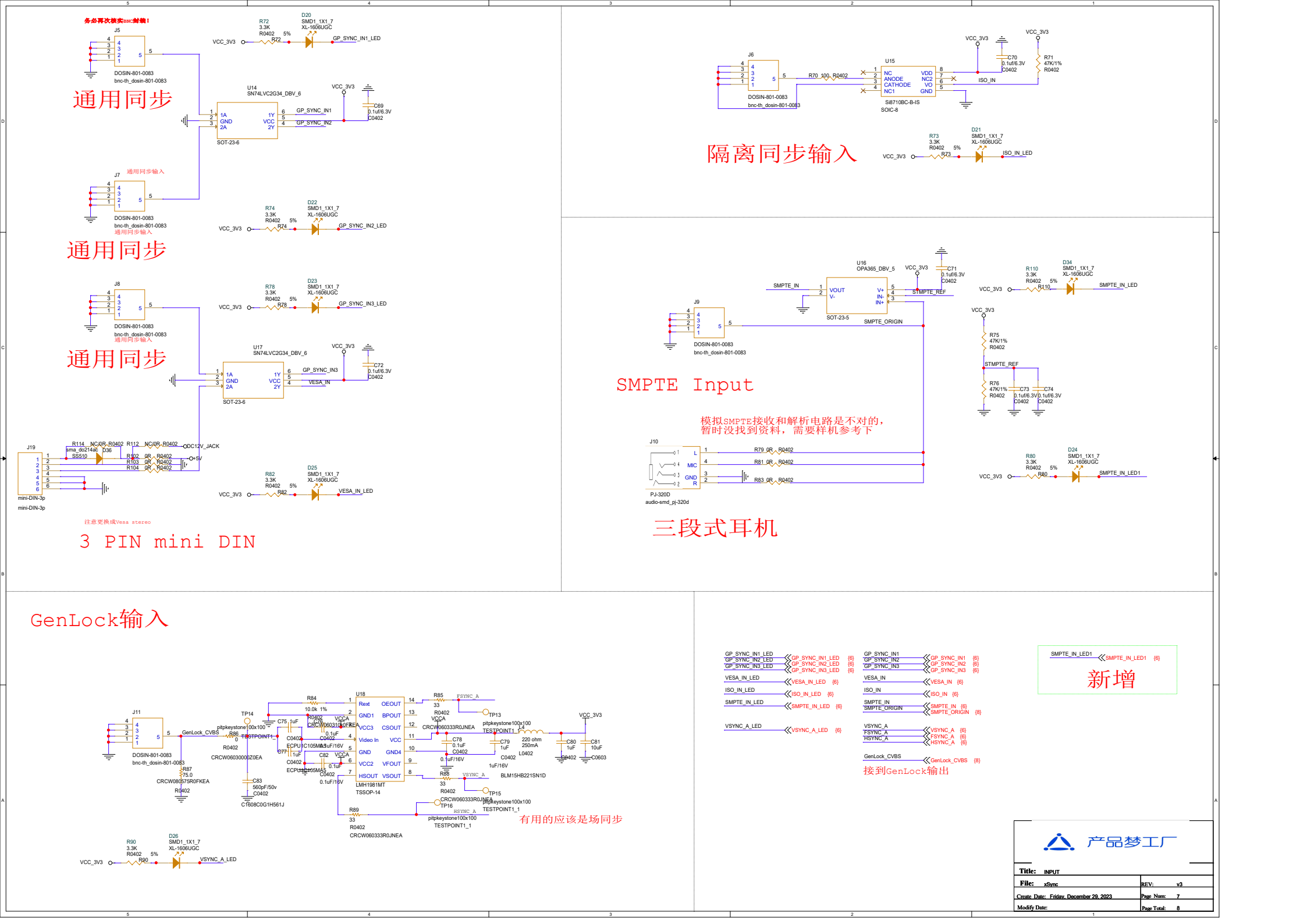
2.54-2*5P简牛（C5665）

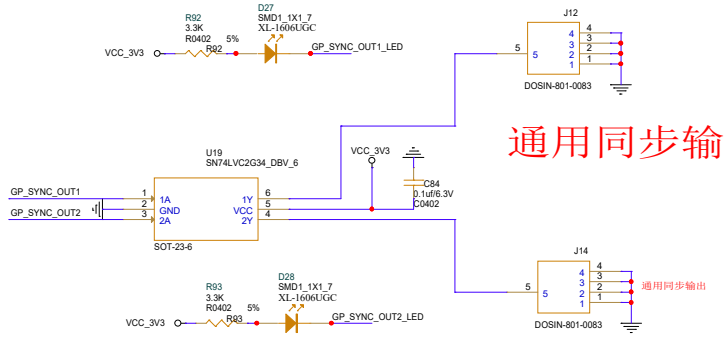




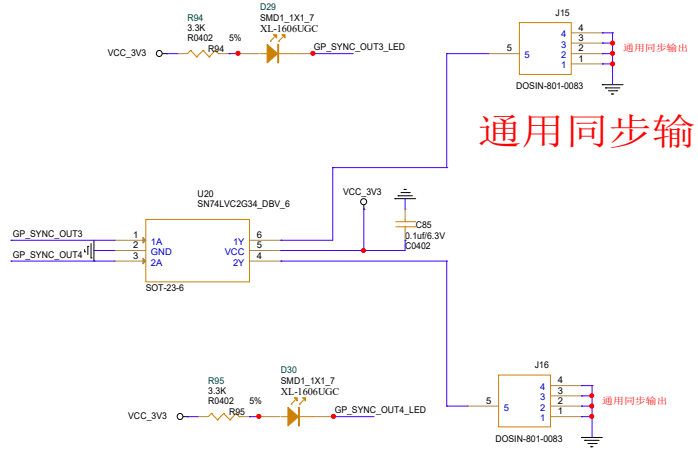
产品梦工厂

Title: FPGA	
File: xSync	**REV:** v3
Create Date: Saturday, October 14, 2023	Page Num: 6
Modify Date:	Page Total: 8


务必再次核实BNC封装！
通用同步
通用同步输入
通用同步
通用同步输入
通用同步
通用同步输入
3 PIN mini DIN
注意更换成Vesa stereo
隔离同步输入
SMPTE Input
模拟SMPTE接收和解析电路是不对的，
暂时没找到资料，需要样机参考下
三段式耳机
GenLock输入
有用的应该是场同步
新增
接到GenLock输出
产品梦工厂
Title: INPUT
File: xSync
REV: v3
Create Date: Friday, December 29, 2023
Page Num: 7
Modify Date:
Page Total: 8

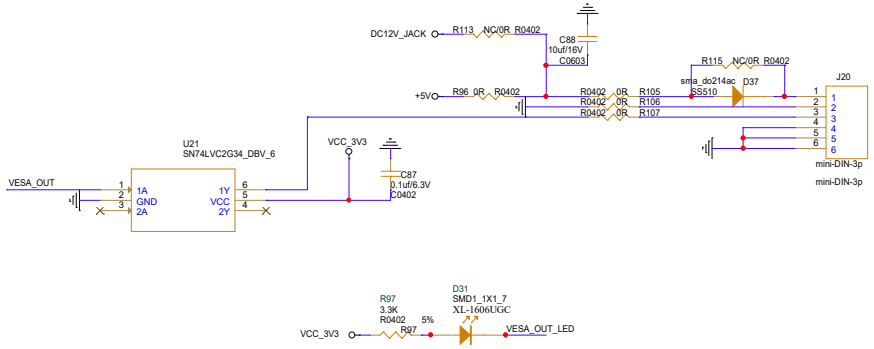


通用同步输出

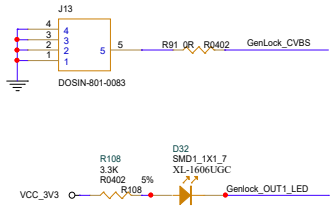


通用同步输出

VESA输出



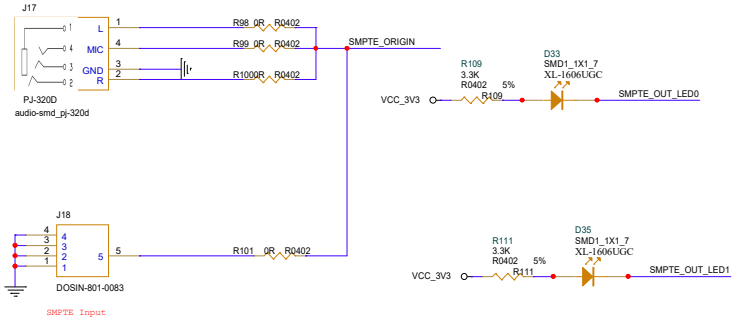
GenLock输出

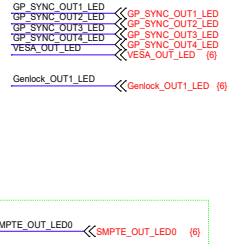


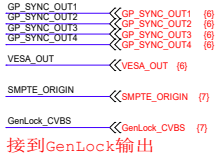
Genlock输出难道还需要视频编码？
还是把输入原封不动的输出？

SMPTE输出

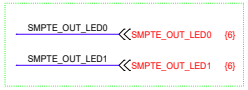
SMPTE输出电路还不会，先原样输出







接到GenLock输出



新增

产品梦工厂

Title:	OUTPUT		
File:	xSync	REV:	v3
Create Date:	Saturday, October 14, 2023	Page Num:	8
Modify Date:		Page Total:	8