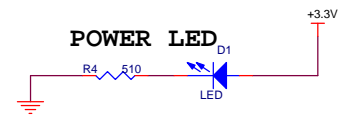
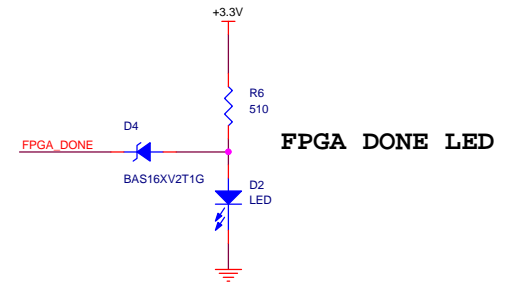
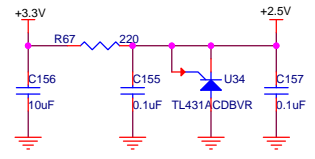
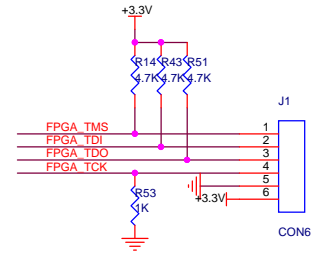
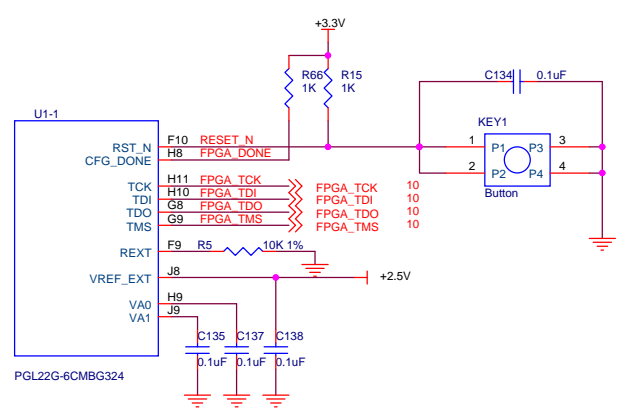
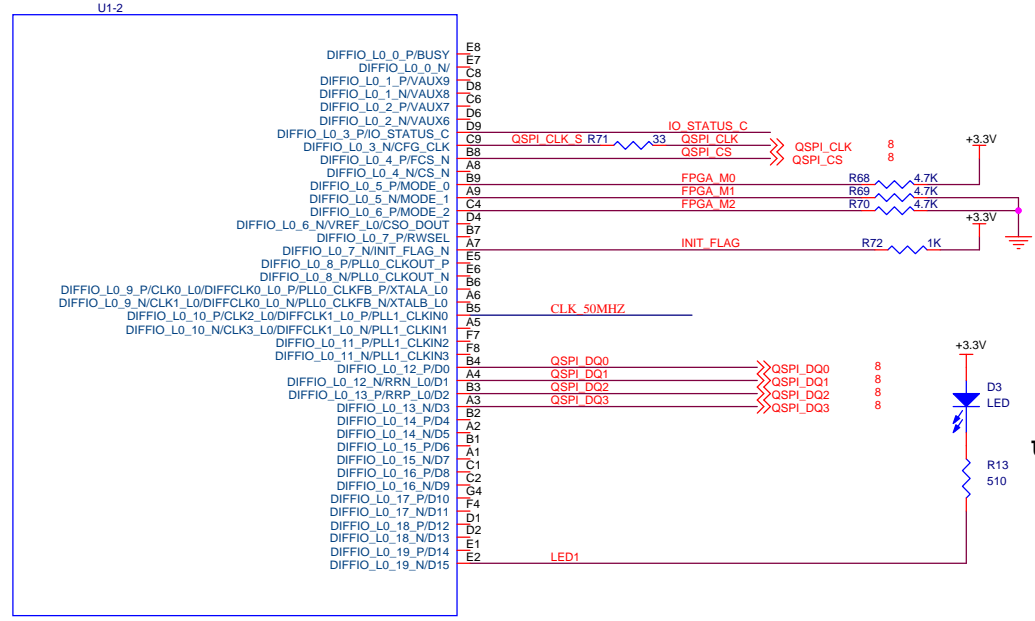
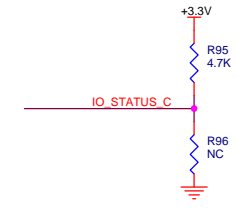
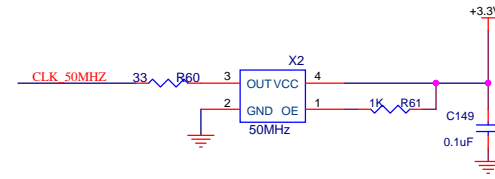


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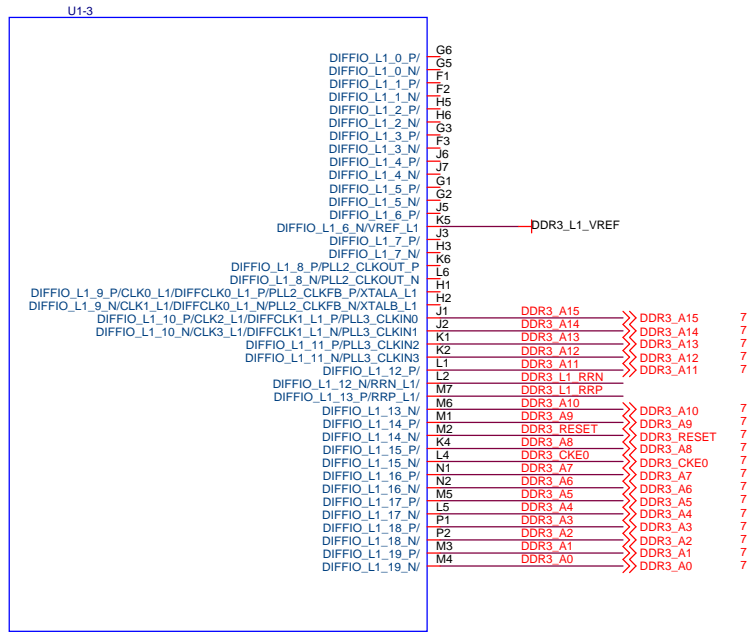




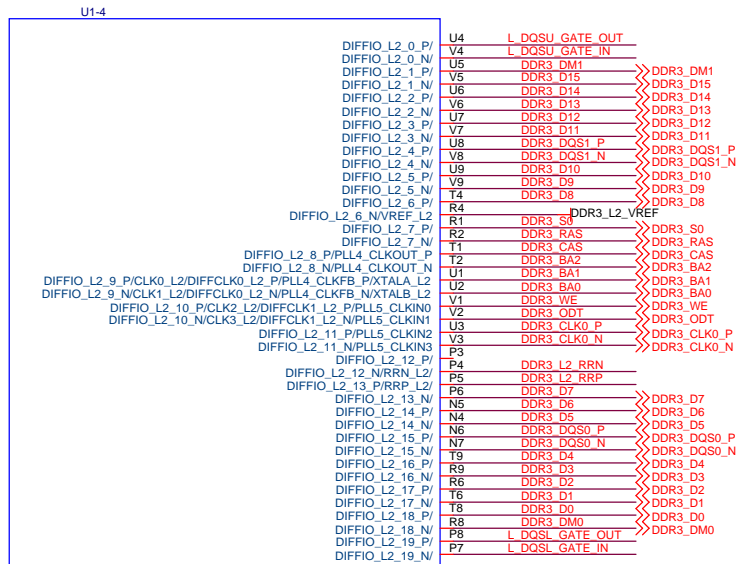
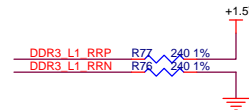
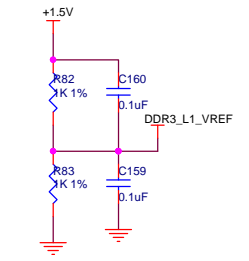
主SPI 模式

USER LED

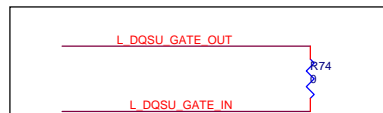
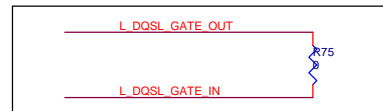
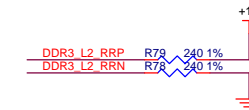
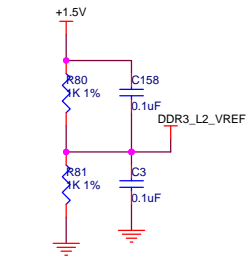
PGL22G-6CMBG324



PGL22G-6CMBG324



PGL22G-6CMBG324



1. 从DDR所在的BANK连出一根线，一直走线到DDR Memory附近，再绕回到DDR所在的BANK
2. 绕线总长度=CK长度+DQ走线长度

U1-5

DIFFIO_R0_0_P/VAUX5	E12	R0 0 P	R0 0 P	10
DIFFIO_R0_0_N/VAUX4	E11	R0 0 N	R0 0_N	10
DIFFIO_R0_1_P/VAUX3	D10	R0 1 P	R0 1_P	10
DIFFIO_R0_1_N/VAUX2	C10	R0 1 N	R0 1_N	10
DIFFIO_R0_2_P/VAUX1	D13	R0 2 P	R0 2_P	10
DIFFIO_R0_2_N/VAUX0	D11	R0 2 N	R0 2_N	10
DIFFIO_R0_3_P/VAUX0	D11	R0 3 P	R0 3_P	10
DIFFIO_R0_3_N/VAUX0	C11	R0 3 N	R0 3_N	10
DIFFIO_R0_4_P/FCFS2_N	B10	R0 4 P	R0 4_P	10
DIFFIO_R0_4_N/BFCE_N	A10	R0 4 N	R0 4_N	10
DIFFIO_R0_5_P/BFOE_N	B11	R0 5 P	R0 5_P	10
DIFFIO_R0_5_N/BADRV0_N	A11	R0 5 N	R0 5_N	10
DIFFIO_R0_6_P/BPFW_E_N	B12	R0 6 P	R0 6_P	10
DIFFIO_R0_6_N/VREF_R0	A12	R0 6 N	R0 6_N	10
DIFFIO_R0_7_P/VS1	B13	FPGA VS1	R0 6_N	10
DIFFIO_R0_7_N/VS0	A13	FPGA VS0	FPGA VS1	8
DIFFIO_R0_8_P/PLLO_CLKIN0	B15	R0 8 P	R0 8_P	10
DIFFIO_R0_8_N/PLLO_CLKIN1	A15	R0 8 N	R0 8_N	10
DIFFIO_R0_9_P/CLK0_R0/DIFFCLK0_R0_P/PLLO_CLKIN2/XTALA_R0	B14	R0 9 P	R0 9_P	10
DIFFIO_R0_9_N/CLK1_R0/DIFFCLK0_R0_N/PLLO_CLKIN3/XTALB_R0	A14	R0 9 N	R0 9_N	10
DIFFIO_R0_10_P/CLK2_R0/DIFFCLK1_R0_P/PLL1_CLKFB_P	B16	R0 10 P	R0 10_P	10
DIFFIO_R0_10_N/CLK3_R0/DIFFCLK1_R0_N/PLL1_CLKFB_N	A16	R0 10 N	R0 10_N	10
DIFFIO_R0_11_P/PLL1_CLKOUT_P	C15	R0 11 P	R0 10_N	10
DIFFIO_R0_11_N/PLL1_CLKOUT_N	D15	R0 11 N	R0 11_P	10
DIFFIO_R0_12_P/D16/ADR0	B17	R0 12 P	R0 12_P	10
DIFFIO_R0_12_N/RRN_R0/D17/ADR1	A17	R0 12 N	R0 12_N	10
DIFFIO_R0_13_P/RRP_R0/D18/ADR2	F11	R0 13 P	R0 13_P	10
DIFFIO_R0_13_N/D19/ADR3	G11	R0 13 N	R0 13_N	10
DIFFIO_R0_14_P/D20/ADR4	E15	R0 14 P	R0 13_N	10
DIFFIO_R0_14_N/D21/ADR5	E16	R0 14 N	R0 14_P	10
DIFFIO_R0_15_P/D22/ADR6	F12	R0 15 P	R0 14_N	10
DIFFIO_R0_15_N/D23/ADR7	G12	R0 15 N	R0 15_P	10
DIFFIO_R0_16_P/D24/ADR8	B18	R0 16 P	R0 15_N	10
DIFFIO_R0_16_N/D25/ADR9	A18	R0 16 N	R0 16_P	10
DIFFIO_R0_17_P/D26/ADR10	C18	R0 17 P	R0 16_N	10
DIFFIO_R0_17_N/D27/ADR11	C17	R0 17 N	R0 17_P	10
DIFFIO_R0_18_P/D28/ADR12	D18	R0 18 P	R0 17_N	10
DIFFIO_R0_18_N/D29/ADR13	D17	R0 18 N	R0 18_P	10
DIFFIO_R0_19_P/D30/ADR14	E18	R0 19 P	R0 18_N	10
DIFFIO_R0_19_N/D31/ADR15	E17	R0 19 N	R0 19_P	10

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U1-6

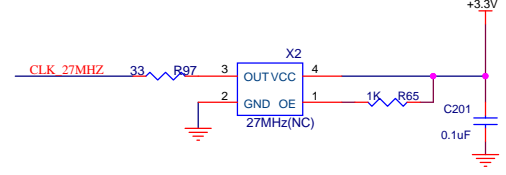
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DIFFIO_R1_1_P/ADR17	F18	R1 1 P	R1 1_P	10
DIFFIO_R1_1_N/ADR18	E17	R1 1 N	R1 1_N	10
DIFFIO_R1_2_P/ADR19	G14	R1 2 P	R1 1_P	10
DIFFIO_R1_2_N/ADR20	G13	R1 2 N	R1 2_P	10
DIFFIO_R1_3_P/ADR21	F16	R1 3 P	R1 2_N	10
DIFFIO_R1_3_N/ADR22	G16	R1 3 N	R1 3_P	10
DIFFIO_R1_4_P/ADR23	H13	R1 4 P	R1 3_N	10
DIFFIO_R1_4_N/ADR24	G18	R1 5 P	R1 4_P	10
DIFFIO_R1_5_P/ADR25	G17	R1 5 N	R1 4_N	10
DIFFIO_R1_5_N/VAUX0	J15	R1 6 P	R1 5_P	10
DIFFIO_R1_6_P/VREF_R1	J14	R1 6 N	R1 5_N	10
DIFFIO_R1_7_P/VAUX0	H16	R1 7 P	R1 6_P	10
DIFFIO_R1_7_N/VAUX0	K14	R1 7 N	R1 6_N	10
DIFFIO_R1_8_P/PLL2_CLKIN0	K16	CLK 27MHZ	R1 7_P	10
DIFFIO_R1_8_N/PLL2_CLKIN1	K15		R1 7_N	10
DIFFIO_R1_9_P/CLK0_R1/DIFFCLK0_R1_P/PLL2_CLKIN2/XTALA_R1	H18	R1 9 P	R1 9_P	10
DIFFIO_R1_9_N/CLK1_R1/DIFFCLK0_R1_N/PLL2_CLKIN3/XTALB_R1	J17	R1 9 N	R1 9_N	10
DIFFIO_R1_10_P/CLK2_R1/DIFFCLK1_R1_P/PLL3_CLKFB_P	J18	R1 10 P	R1 9_N	10
DIFFIO_R1_10_N/CLK3_R1/DIFFCLK1_R1_N/PLL3_CLKFB_N	J17	R1 10 N	R1 10_P	10
DIFFIO_R1_11_P/PLL3_CLKOUT_P	K18	R1 11 P	R1 10_N	10
DIFFIO_R1_11_N/PLL3_CLKOUT_N	K17	R1 11 N	R1 11_P	10
DIFFIO_R1_12_P/VAUX0	L18	R1 12 P	R1 11_N	10
DIFFIO_R1_12_N/RRN_R1/VAUX0	L17	R1 12 N	R1 12_P	10
DIFFIO_R1_13_P/RRP_R1/VAUX0	L13	R1 13 P	R1 12_N	10
DIFFIO_R1_13_N/D19/ADR3	L12	R1 13 N	R1 13_P	10
DIFFIO_R1_14_P/D20/ADR4	L16	R1 14 P	R1 13_N	10
DIFFIO_R1_14_N/D21/ADR5	M16	R1 14 N	R1 14_P	10
DIFFIO_R1_15_P/D22/ADR6	M13	R1 15 P	R1 14_N	10
DIFFIO_R1_15_N/D23/ADR7	M14	R1 15 N	R1 15_P	10
DIFFIO_R1_16_P/D24/ADR8	M18	R1 16 P	R1 15_N	10
DIFFIO_R1_16_N/D25/ADR9	M17	R1 16 N	R1 16_P	10
DIFFIO_R1_17_P/D26/ADR10	N18	R1 17 P	R1 16_N	10
DIFFIO_R1_17_N/D27/ADR11	N17	R1 17 N	R1 17_P	10
DIFFIO_R1_18_P/D28/ADR12	N15	R1 18 P	R1 17_N	10
DIFFIO_R1_18_N/D29/ADR13	N16	R1 18 N	R1 18_P	10
DIFFIO_R1_19_P/D30/ADR14	L15	R1 19 P	R1 18_N	10
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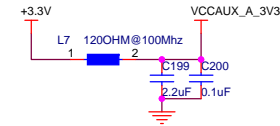
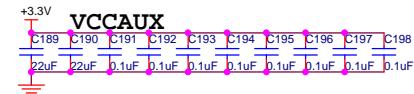
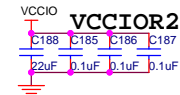
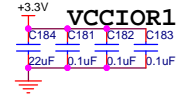
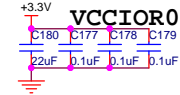
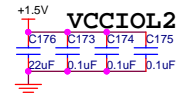
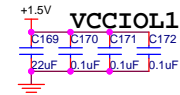
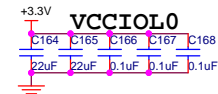
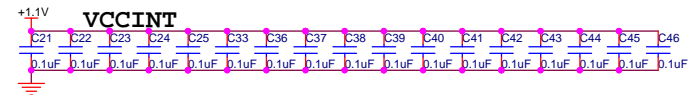
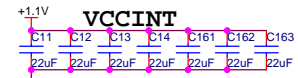
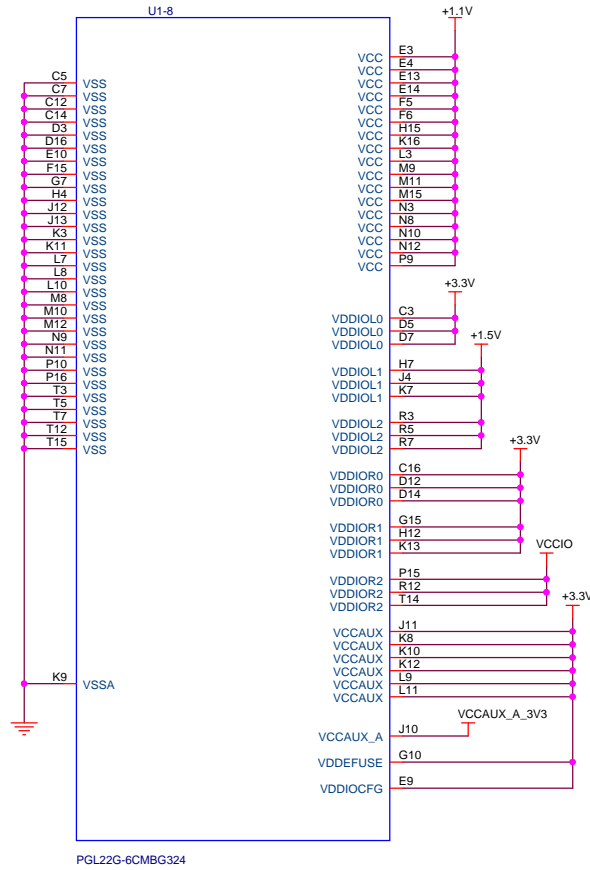
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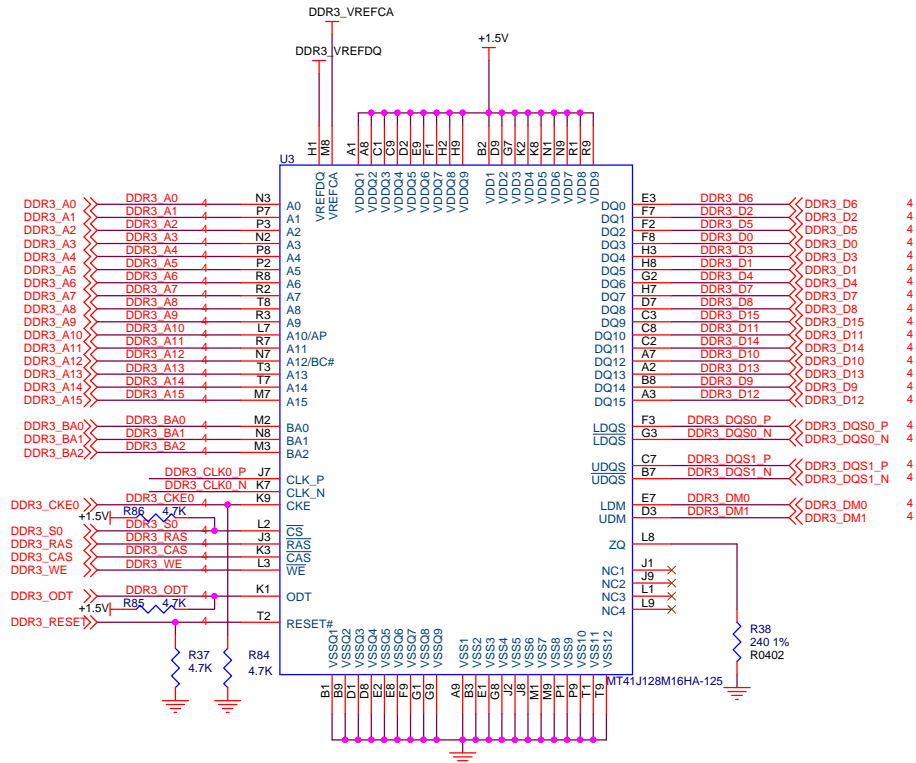
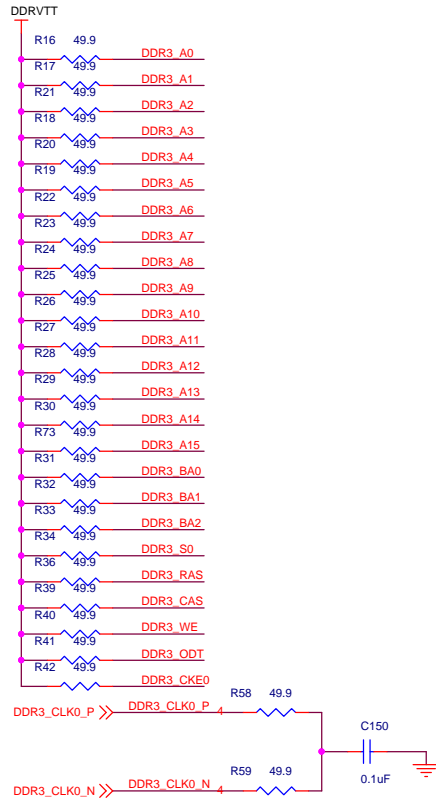
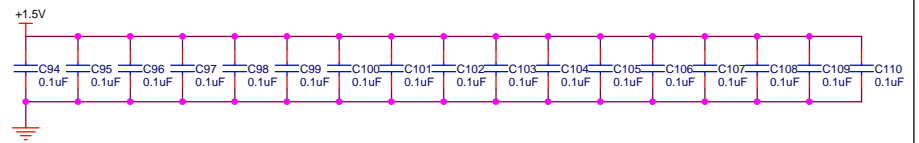
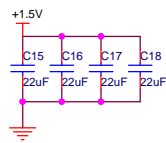
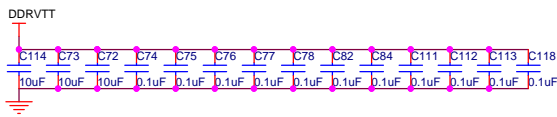
U1-7

DIFFIO_R2_0_P/VAUX5	R10	R2 0 P	R2 0_P	10
DIFFIO_R2_0_N/VAUX4	T10	R2 0 N	R2 0_N	10
DIFFIO_R2_1_P/VAUX3	U10	R2 1 P	R2 1_P	10
DIFFIO_R2_1_N/VAUX2	U13	R2 2 P	R2 1_N	10
DIFFIO_R2_2_P/VAUX1	V13	R2 2 N	R2 2_P	10
DIFFIO_R2_2_N/VAUX0	U12	R2 3 P	R2 2_N	10
DIFFIO_R2_3_P/VAUX0	V12	R2 3 N	R2 3_P	10
DIFFIO_R2_3_N/VAUX0	U11	R2 4 P	R2 3_N	10
DIFFIO_R2_4_P/VAUX0	V11	R2 4 N	R2 4_P	10
DIFFIO_R2_4_N/VAUX0	R11	R2 5 P	R2 4_N	10
DIFFIO_R2_5_P/VAUX0	T11	R2 5 N	R2 5_P	10
DIFFIO_R2_5_N/VAUX0	P11	R2 6 P	R2 5_N	10
DIFFIO_R2_6_P/VREF_R2	P12	R2 6 N	R2 6_P	10
DIFFIO_R2_7_P/VAUX0	V17	R2 7 N	R2 6_N	10
DIFFIO_R2_7_N/VAUX0	U18	R2 8 P	R2 7_P	10
DIFFIO_R2_8_P/PLL4_CLKIN0	U17	R2 8 N	R2 7_N	10
DIFFIO_R2_8_N/PLL4_CLKIN1	T18	R2 9 P	R2 8_P	10
DIFFIO_R2_9_P/CLK0_R2/DIFFCLK0_R2_P/PLL4_CLKIN2/XTALA_R2	T17	R2 9 N	R2 8_N	10
DIFFIO_R2_9_N/CLK1_R2/DIFFCLK0_R2_N/PLL4_CLKIN3/XTALB_R2	R17	R2 10 P	R2 9_N	10
DIFFIO_R2_10_P/CLK2_R2/DIFFCLK1_R2_P/PLL5_CLKFB_P	R18	R2 10 N	R2 10_P	10
DIFFIO_R2_10_N/CLK3_R2/DIFFCLK1_R2_N/PLL5_CLKFB_N	P17	R2 11 P	R2 10_N	10
DIFFIO_R2_11_P/PLL5_CLKOUT_P	P18	R2 11 N	R2 11_P	10
DIFFIO_R2_11_N/PLL5_CLKOUT_N	R16	R2 12 P	R2 11_N	10
DIFFIO_R2_12_P/D16/ADR0	T16	R2 12 N	R2 12_P	10
DIFFIO_R2_12_N/RRN_R2/D17/ADR1	U14	R2 13 P	R2 12_N	10
DIFFIO_R2_13_P/RRP_R2/D18/ADR2	V14	R2 13 N	R2 13_P	10
DIFFIO_R2_13_N/D19/ADR3	U15	R2 14 P	R2 13_N	10
DIFFIO_R2_14_P/D20/ADR4	V15	R2 14 N	R2 14_P	10
DIFFIO_R2_14_N/D21/ADR5	U16	R2 15 P	R2 14_N	10
DIFFIO_R2_15_P/D22/ADR6	R14	R2 16 P	R2 15_P	10
DIFFIO_R2_15_N/D23/ADR7	R15	R2 16 N	R2 15_N	10
DIFFIO_R2_16_P/D24/ADR8	R13	R2 17 P	R2 16_P	10
DIFFIO_R2_16_N/D25/ADR9	T13	R2 17 N	R2 16_N	10
DIFFIO_R2_17_P/D26/ADR10	P13	R2 18 P	R2 17_P	10
DIFFIO_R2_17_N/D27/ADR11	P14	R2 18 N	R2 17_N	10
DIFFIO_R2_18_P/D28/ADR12	N13	R2 19 P	R2 18_P	10
DIFFIO_R2_18_N/D29/ADR13	N14	R2 19 N	R2 18_N	10
DIFFIO_R2_19_P/D30/ADR14				
DIFFIO_R2_19_N/D31/ADR15				

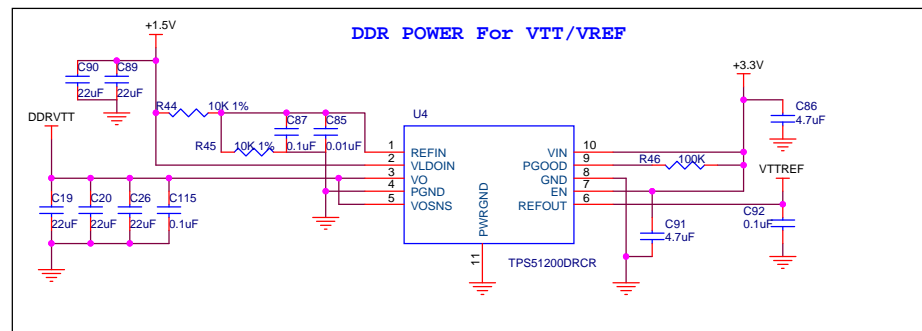
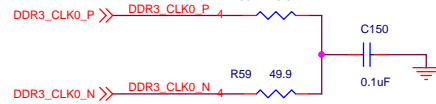
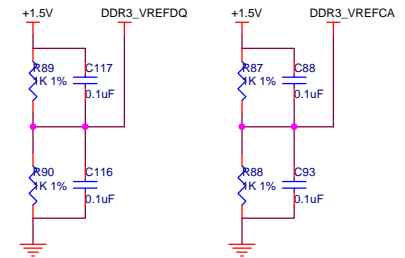
PGL22G-6CMBG324



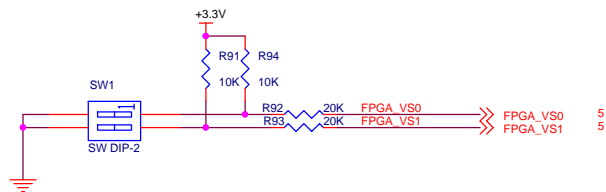
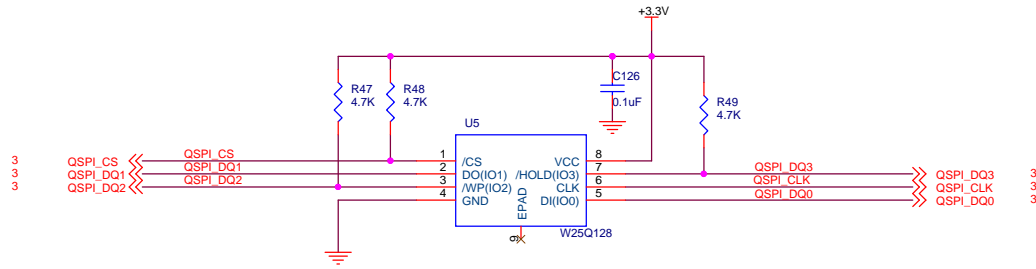




**Close to DDR**

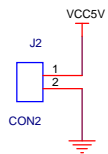


## FPGA CONFIG SPI



FPGA_VS0	FPGA_VS1	Boot Mode
0	0	选择第一套数据流
0	1	选择第二套数据流
1	0	选择第三套数据流
1	1	选择第四套数据流





POWER ON: VCCINT(1.0V)->VCCBRAM(1.0V)->VCCAUX-(1.8V)>VCCO(1.5V and 3.3V)

